Novel Bonding and Joining Technology for Power Electronics

- Enabler for improved lifetime, reliability, cost and power density

用于电力电子的新型焊接和连接技术

- 可延长生命周期、提高可靠性、降低成本和加大功率密度

Abstract

摘要

An increase in reliability and life time for power semiconductors at the same or lower cost remain high on the wish list for many Power Electronics Engineers. Ideally all of these improvements combined with the potential for higher power density.

对功率半导体而言，提高可靠性、延长生命周期，而成本保持不变或更低，这一直是很多电力电子工程师的不懈追求。从理论上说，所有这些改进都取决于高功率密度的潜力。

Even though the semiconductors themselves continuously improve in current density year over year, the thermal stack and the associated bonding and joining technology remain the limiting factor. This is especially true when looking at the potential of SiC or GaN semiconductors.

随着时间的推移，即使半导体本身能持续改进电流密度，热堆栈及相关焊接和连接技术仍然是制约因素。当综合判断碳化硅（SiC）或氮化镓（GaN）的潜力时，尤其如此。

This paper presents a solution for a highly reliable power module: an interconnect technology with outstanding reliability is achieved while maintaining the highly desired design flexibility of heavy wire bonding technology. For the presented solution, die attach is performed by a low pressure sintering process. The top side interconnects are achieved by using three innovative solutions: a sinterable top metallization, a metal buffer plate joined on top of the chip metallization (Danfoss Bond Buffer – DBB) and finally Cu wire bonds.

本文提出了一种高可靠性的功率模块解决方案，即一种可靠性特别高同时可保持粗线绑定技术较高的设计灵活性的互连技术。对于本文提出的解决方案而言，采用低压烧结工艺，可完成晶粒粘着。通过以下三种创新解决方案，可实现顶层互连：可烧结顶层金属化、采用与芯片金属化顶层相连接的金属缓冲板（丹佛斯粘合缓冲板— DBB），最后用铜线连接。

1. Introduction

1.引言

State of the art in bonding and joining technology for power modules is the use of a void- and lead free solder process for the interconnect of the bottom side of the semiconductor to the substrate and Aluminum (Al) heavy wire for the top side interconnect. Al wire bonding has become the top side interconnect of choice for its high level of design flexibility and its simplicity when it comes to automation. Unfortunately Al heavy wire bonding has become a bottle neck in many designs due to its well-known life time limitations.

功率模块焊接和连接的最新技术水平是空白的使用——半导体底面与顶层基材和铝（Al)粗线互连的无铅焊接工艺。由于设计灵活性大、实现自动化的程序简单，铝线绑定现在已成为顶层互连的首选。遗憾的是，由于众所周知的生命周期局限的原因，铝粗线焊接成了众多设计的瓶颈。

In the past some solutions for chip top contacts based on sintered ribbons or braided tapes were presented [1][2]. Copper (Cu) wire bonding has seen a high adaption rate as a replacement for Gold (Au) wire heavy for IC's or memory products. It is also highly desirable in larger diameters as a replacement for Aluminum and some work on this subject has been presented [4]. Cu wire bonding maintains the design

地址：深圳市南山区科技园科技路 1 号桑达科技大厦东裙楼二楼，Tel/Fax: 0755-82784916/82784906, E-mail: Samuelsha@dmaxtech.cn，
Http: www.dmaxtech.cn

and process flexibility of the current Al wire bonding method but heavy Cu wires requires a much more robust top metallization in order to protect the power semiconductor against chip crack and damage of the fine structures under the bond pad. Many power semiconductor manufacturers are working on possible solutions for this problem.

过去，利用烧结带或编织带提出了一些关于芯片顶层触点的解决方案[1][2]。对于IC或存储产品而言，作为粗金（Au）线的替代品，铜（Cu）线绑定具有较高的适配率。还强烈希望采用较大直径的电线作为铝线的替代品，并提出了此课题的有关事项[4]。铜线绑定保持了当前铝线绑定法的设计灵活性和工艺灵活性，但是粗铜线要求顶层金属化整体更加牢固，以防止功率半导体在粘合焊盘的作用下出现芯片裂纹和结构损坏。很多功率半导体制造厂正在着手解决这一问题。

One of the key advantages of the proposed joining method is that it enables the use of heavy Cu wire bonding and does not require a change of the top metallization of semiconductors. It allows the semiconductor manufacturers to rely on established process technologies and metallization already established and it keeps the dividing line between front-end and back-end/packaging. With that a faster time-to-market for high-reliable power modules is made possible.

本文提出的连接方法的主要优势之一是这种方法可使用粗铜线绑定，无需改变半导体顶层金属化。因此，半导体制造厂可依靠现有的工艺技术和既定的金属化，在前端和后端/封装材料之间留出分隔线。于是，高可靠性功率模块完全有可能实现较快的上市时间。

Silver sintering is already established as a highly reliable bonding and joining technology for power semiconductors. It requires well-known metallization surfaces such as NiAu, Pd or Ag. All of these surfaces are common and already available from most manufacturers.

银烧结是一种成熟的功率半导体焊接和连接技术，可靠性很高，要求使用常见的金属化表面。例如NiAu, Pd或Ag，这些表面都很常用，大多数制造厂有售。

2. Bonding and Joining Technologies

2.绑定和焊接技术

2.1. Low Pressure Sintering

2.1. 低压烧结

Low pressure sintering technology was applied to produce rectifier power modules. This technology assures better quality for power modules in terms of thermal, mechanical and electrical properties. The sintering process is performed by applying silver paste between the parts to be joined. During the sintering process the pressure provides a dense silver layer which is needed for reliable joints. This pressure could be reduced when silver particles and organics in the sinter paste actively contribute to increasing the diffusion forces during the sintering process. Current sintering processes can be performed at pressure levels noticeable below 40MPa as reported in the past [6][7]. The reduction of pressure allows producing modules with different die thicknesses and sizes thus increasing the design flexibility and opening the technology for mass production.

低压烧结接受用于生产整流器功率模块，采用这种技术，功率模块质量更好，热工特性、机械特性和电气特性优良。烧结时需要在焊接件之间涂银膏。烧结过程中，施加压力产生一层密实的银层，连接可靠。烧结过程中，当银膏中的银颗粒和有机物促使扩散力增加时，可减小施加的压力。据报道，当前的烧结工艺可在40 MPa以下的压力水平完成[6][7]。减小压力可生产不同规格的模块，从而增加设计灵活性，便于利用批量生产技术。

2.2. Heavy Cu Wire Bonding

2.2.粗铜线绑定

地址：深圳市南山区科技园科技路 1 号桑达科技大厦东裙楼二楼，Tel/Fax: 0755-82784916/82784906, E-mail: Samuelsha@dmaxtech.cn，
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Copper wire bonding is one of the most promising technologies for connecting high current interconnections in power electronics assemblies. The high flexibility in the layout and established quality processes from the aluminum wire bonding are only two reasons to promote the development of Cu wire bonding. The copper material for wire bond interconnections provides mainly two benefits over aluminum, an increase in current capacity by 37% and the excellent thermal conductivity of copper (~80% better compared to Al).

铜线绑定是电力电子产品总成的大电流互连最看好的技术之一。与铝线绑定相比，铜线绑定布局灵活性高、质量过程成熟，正因为这两条原因，加快了铜线绑定的研发。与铝材相比，电线粘合互连采用铜质材料，有两大好处：1. 电流能力增加37%；2. 铜的热传导率好（比铝的热传导率高达80%）。

2.3. Danfoss Bond Buffer Technology (DBB)

2.3. 丹佛斯粘合缓冲板技术（DBB）

The Danfoss Bond Buffer Technology (DBB) consists of a thin copper foil which is sintered onto the top metallization surface of the semiconductor (Fig. 11). Furthermore the same sintering technology is also used to replace the solder interconnect for the bottom side interface of the semiconductor to the DBC substrate.

丹佛斯粘合缓冲板技术（DBB）由烧结在金属半导体顶层金属化表面上的薄铜箔组成（图11）。此外，替换半导体底面接口与DBC基体的凸点互连时，也可采用相同的烧结技术。

The design of the DBB is dimensioned for the thermo mechanical optimum to reduce the mechanical stress due to CTE mismatch. In addition to the property during Cu wire bonding to absorb energy and protect the die, the DBB also offers thermal and electrical advantages. DBB provides a uniform current density distribution in the semiconductor. Due to the improved vertical current flow, there is no mandatory need to place a stitch bond on the semiconductor.

设计DBB时，其尺寸要保证热机械优化，以减小由于CTE不匹配而引起的机械应力。除了铜线绑定期间可吸收能量和保护晶片的特性外，DBB还具有很多热特性和电气特性优势。采用DBB后，半导体内出现均匀的电流密度分配。由于竖向电流流动得到改善，无需在半导体上采用针脚式粘合。

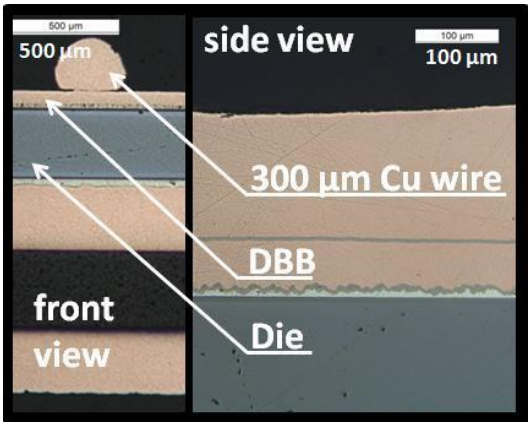

Fig. 1. Cross section of a DBB Ag sintered and Cu wire bonded thermal stack

图1 烧结DBB银和铜线绑定热堆栈的横截面

This section will further show a direct comparison between a standard rectifier module and the same module utilizing all three in section 2 presented methods.

此部分将进一步介绍标准整流器模块和第2部分所述方法制成的相同模块之间的直接比较结果。

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3. Results
3. 结果
3.1. Thermal Simulations
3.1. 热模拟

To demonstrate the performance of the new packaging technology, different design concepts were investigated using thermal simulation software FlowEFD. All concepts follow the same conditions in order to compare the results. Fig. 22 shows the boundary conditions of the FEM simulations.

为了证明新封装技术的性能，我们使用热模拟软件FlowEFD，对不同的设计方案进行了研究。为了便于对结果进行比较，所有方案都采用相同的条件。图22显示的是FEM模拟的边界条件.

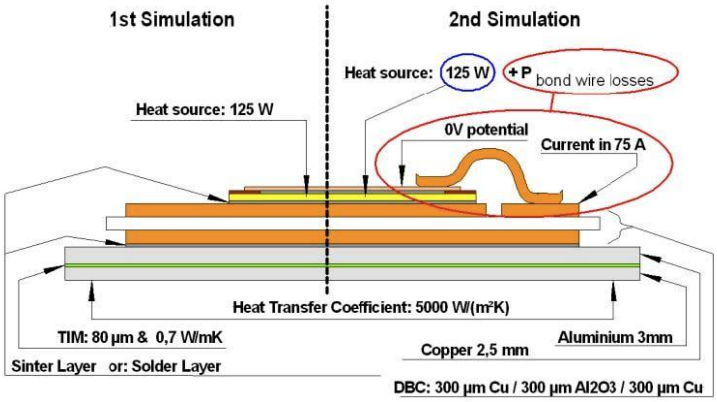

Fig. 2. The boundary conditions for first and second simulation part

图2 第一模拟部分和第二模拟部分的边界条件

The additional thermal capacity of the DBB has a positive effect on the Zth curve, because it is able to store short thermal energy pulses. Fig. 3 shows the thermal impedance of the different variants (V1 – V5) at different times (10ms, 100ms, 1000ms). In the sintered DBB variant (V5) the Zth at 10ms was lower by about 22%, than in the soldered standard technology (V1). Moreover the thermal capacity of the DBB has no negative impact on the Rth, because it is not in the thermal path between the heat source (die) and the heat sink.

DBB的附加热能力对Zth曲线有积极影响，因为它能储存短热能脉冲。图3所示的是不同变型(V1～V5)不同时间（10 ms、 100 ms、1000 ms）的热阻抗。在烧结的DBB变型（V5）中，10 ms的Zth比标准焊机技术 (V1)低大于22%。另外，DBB的热能力对Rth没有负面影响，因为它未在热源（晶片）和热沉之间的传热路径上。

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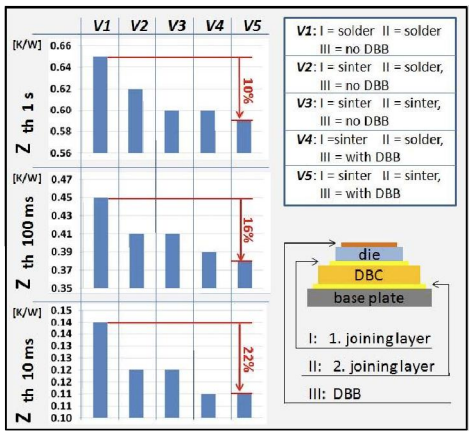

Fig. 3. Thermal impedance (1st simulation) at different times for five different packaging options

图3 五种不同封装方法不同时间的热阻抗（第一次模拟）

3.2. Reliability

3.2.可靠性

Comparison data were taken from previous tests of standard soldered module, sintered module and braided tape module [2]. The power cycling results are presented in Fig. 4. The standard Danfoss rectifier module gained about 40.000 cycles and the sintered modules with Al wires about 70.000 cycles. The DBB modules reached at least 600.000 cycles, **it means about 15 times better than standard Danfoss module** and about 60 times better than industry standard [11].

从以前的标准焊接模块、烧结模块和编织带模块试验中得出比较数据 [2]。功率循环结果如图4所示。丹佛斯标准整流器模块约有40,000个循环，而采用铝线的烧结模块约有70,000个循环。DBB模块至少有600,000个循环，**比丹佛斯标准模块好约15倍**，比行业标准好约60倍[11]。

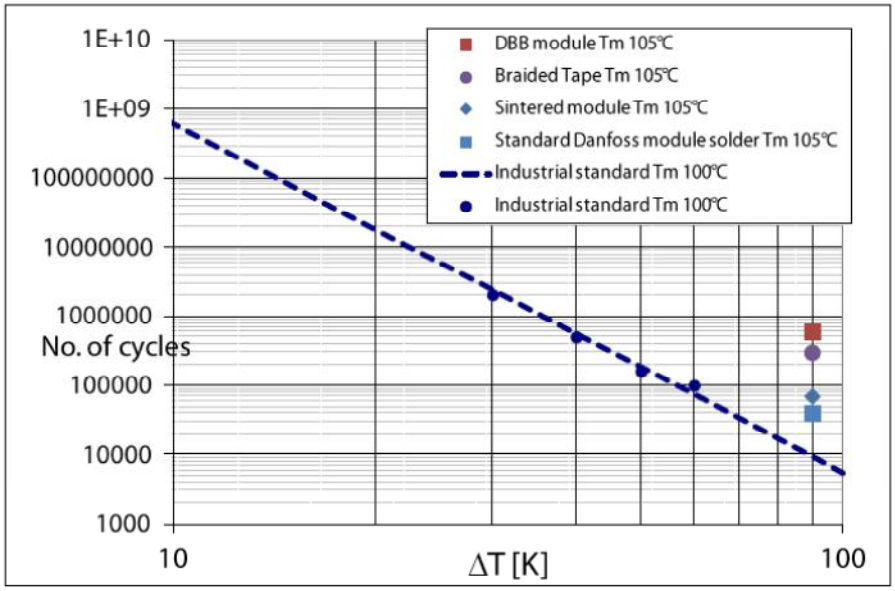

Fig. 4. Active power cycling results for DBB module and benchmark modules.

图4 DBB模块和基准模块的有功功率循环结果

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4. Conclusions
4. 结论

Introducing the Danfoss Bond Buffer (DBB) technology enables Cu heavy wire bonding and is completely compatible with the highly reliable Ag sinter process. The result is a highly robust power module that is at least a factor of 15 more durable than the comparable standard module and factor of 60 then industry standard.

引入丹佛斯焊接缓冲板（DBB）技术，可采用粗铜线绑定，完全与可靠性高的银烧结工艺兼容。结果是功率模块整体十分牢固，耐久性是同类标准模块的至少15倍，是行业标准的60倍。

With the introduction of heavy Cu bonding for semiconductors by using the Danfoss Bond Buffer it is now possible to combine a number of benefits in the new generation of power modules:

使用丹佛斯焊接缓冲板，半导体采用粗铜线绑定后，现在可制作出新一代功率模块，其主要益处如下：

- heavy copper wires can be bonded on chips
- additional thermal capacity for better Zth is added without increasing the Rth
- extra cooling by Cu-wires leads to higher lifetime or higher current density
- extended lifetime is achieved by using sintering techniques between silicon die and DBC substrate
- applicable on all common solderable chip top metallization
- 芯片上可绑定粗铜线。
- 增加 Z_{th} 的附加热能力，而不增加R_{th}。
- 铜线采用特别的冷却方式，生命周期更长或电流密度更大。
- 硅片和DBC基体之间采用烧结技术，可延长使用寿命。
- 适用于所有常见的芯片顶层金属化。

This will allow a short time-to-market with a new technology with extreme benefits by only small impacts to established and trusted ways of manufacturing.

采用新技术，还可缩短上市时间，最大好处是对现有已成熟并值得信赖的制造方式的影响很小。

5. Outlook
5. 前景展望

The next step in development is the DBB-application on transistor layouts using a gate pad area and an emitter area (in case of an IGBT) in the same bond buffer. This will extend the beneficial properties also to the gate wire bond. IGBTs as well as MOSFETs are already under first examinations. Extreme current carrying capability can be enabled due to expanded wire cross sections up to 600µm of each Cu wire.

下一步研发工作是在相同的粘合缓冲板上，使用一个门区域（gate pad area）和一个发射区域（如果是IGBT），在晶体管布局上应用DBB，还将增加门线粘合的有益特性。IGBT和MOSFET已经正在初步检测中。由于每根铜线的横截面增大至600 µm，可达到极端载流能力。

6. Literature
6. 参考文献

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